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Ti–Sb–Te Alloy: A Candidate for Fast and Long-Life Phase-Change Memory

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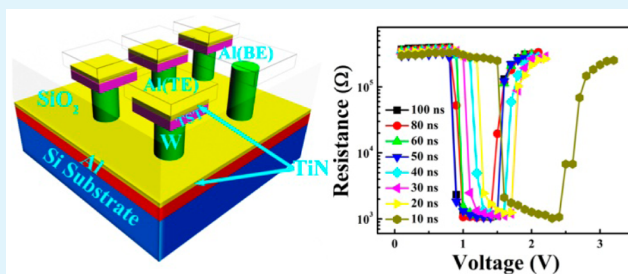
Supporting Information

ABSTRACT: Phase-change memory (PCM) has great potential for numerous attractive applications on the premise of its high-device performances, which still need to be improved by employing a material with good overall phase-change properties. In respect to fast speed and high endurance, the Ti–Sb–Te alloy seems to be a promising candidate. Here, Ti-doped Sb_2Te_3 (TST) materials with different Ti concentrations have been systematically studied with the goal of finding the most suitable composition for PCM applications. The thermal stability of TST is improved dramatically with increasing Ti content. The small density change of $T_{0.32}Sb_2Te_3$ (2.24%), further reduced to 1.37% for $T_{0.56}Sb_2Te_3$, would greatly avoid the voids generated at phase-change layer/electrode interface in a PCM device. Meanwhile, the exponentially diminished grain size (from ~200 nm to ~12 nm), resulting from doping more and more Ti, enhances the adhesion between phase-change film and substrate. Tests of TST-based PCM cells have demonstrated a fast switching rate of ~10 ns. Furthermore, because of the lower thermal conductivities of TST materials, compared with Sb_2Te_3-based PCM cells, $T_{0.32}Sb_2Te_3$-based ones exhibit lower required pulse voltages for Reset operation, which largely decreases by ~50% for $T_{0.43}Sb_2Te_3$-based ones. Nevertheless, the operation voltages for $T_{0.56}Sb_2Te_3$-based cells dramatically increase, which may be due to the phase separation after doping excessive Ti. Finally, considering the decreased resistance ratio, $Ti_xSb_2Te_3$ alloy with x around 0.43 is proved to be a highly promising candidate for fast and long-life PCM applications.



KEYWORDS: *Ti–Sb–Te, Sb_2Te_3, $Ge_2Sb_2Te_5$, phase-change material, high endurance, fast speed*

1. INTRODUCTION

Phase-change memory (PCM), based on rapid and reversible electrothermal-induced phase-change materials, has been widely regarded as one of the most likely candidates in next-generation nonvolatile memory technology.[1] The common phase-change materials utilized in PCM are chalcogenide alloys. These chalcogenide alloys show a pronounced change of electrical properties accompanied by reversible structure change between amorphous (high-resistance) and crystalline (low-resistance) phases.[2] To drive a chalcogenide material into the amorphous state (Reset operation), an electrical pulse of large amplitude is employed and then abruptly cut off to melt-quench the material. In contrast, to realize the crystalline state (Set operation), the material is heated by a wider pulse of lower amplitude to a temperature above the crystallization temperature, while remaining below the melting point.

Having been widely used in commercial DVD-RAM,[3] phase-change material $Ge_2Sb_2Te_5$ (GST) attracts great expectation on application in PCM. However, so far, its high required Reset current (~700 μA at 180 nm node[4]) and relatively low crystallization speed (~50 ns for a cell with 300 nm wide W heating electrode[5]) are the major obstacles of GST-based PCM development. Even though these issues can be alleviated by shrinking the feature size to nanoscale,[6,7] some new problems come along. The most serious one is the accompanying large current density (>40 MA/cm^2),[8] which is far beyond the maximum tolerable current density (~8 MA/cm^2) for wires in large-scale integrated circuit (LSIC).[9]

Recently, PCM cells using Ti–Sb–Te (TST) alloy have been reported to possess 1 order magnitude faster storage speed and ~80% smaller Reset current than the GST-based one, which seems to have more advantages to realize DRAM-like device applications.[10] However, to achieve an overall performance, many other factors should be taken into account: (1) amorphous state should have good thermal stability in order to guarantee data reliability of the memory; (2) density

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variation between amorphous and crystalline phases should be small enough to avoid the presence of void and then to obtain a long-life device; (3) a relatively low thermal conductivity is needed to enhance thermal efficiency; (4) small grain size is also expected to improve the gap-fill capability for high aspect ratio structure; (5) a large resistance ratio helps to distinguish the high/low resistance sensitively and to ensure the accuracy of stored data. Therefore, in this paper, these important parameters of TST with different Ti concentrations are systematically studied, which will help us to find the optimal components and finally to fabricate a competitive PCM with high device performances.

2. EXPERIMENTAL SECTION

TST films with different Ti contents were deposited on SiO_2/Si substrates by an radio frequency (RF) sputtering method with two targets of Ti and Sb_2Te_3 (ST). Components of them were identified by energy-dispersive X-ray spectrometry (EDX) as $Ti_{0.32}Sb_2Te_3$ ($T_{0.32}$ST), $Ti_{0.43}Sb_2Te_3$ ($T_{0.43}$ST), and $Ti_{0.56}Sb_2Te_3$ ($T_{0.56}$ST). Pure ST film was also prepared for comparison. The sheet resistance–temperature (*RT*) curves and thermal stability of these samples were studied by Linkam LMP 95 hot stage. The carrier density and mobility were determined using a homemade Hall system with Keithley 2000 and Keithley 2400 in the magnetic field intensity of 0.5 T. The X-ray reflectivity (XRR) experiment (Burker D8 Discover) was employed to test the density change before and after the crystallization of ∼40 nm thickness films. Au (∼100 nm)/ST or TST (∼200 nm)/Si structures were prepared to measure the thermal conductivities of ST and TST films using a transient thermoreflectance (TTR) technique.[11] Twenty nanometer thickness ST and TST films were directly deposited on supporting grids and were annealed at 250 °C for 2 min. Then, the microstructures of these samples were studied by transmission electron microscope (TEM) analysis using FEI Tecnai F20 operated at 200 kV.

A T-shaped PCM device with a bottom electrode diameter of ∼200 nm was fabricated using 0.13 μm CMOS device fabrication processes. A cross-sectional sample of a PCM cell, as shown in Figure 1, was prepared by employing a focused ion beam (FIB, Nova 200 Nanolab). The device performances, including resistance–voltage and endurance, were characterized by a parameter analyzer (Keithley 2400C) and a pulse generator (Tektronix AWG5002B).

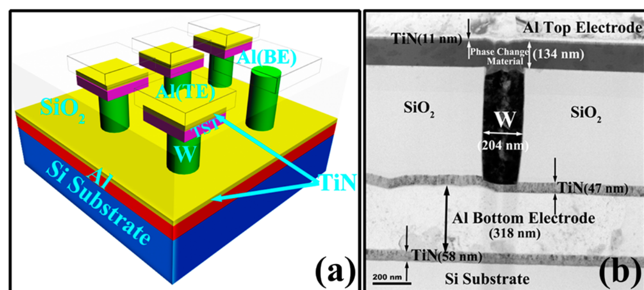

Figure 1. (a) Schematic diagram of a PCM device array. (b) Cross-sectional TEM image of a PCM test cell. The diameter of the bottom W heat electrode is ∼200 nm. TiN film (∼10 nm) is deposited between phase-change film and Al (∼300 nm) top electrode to strengthen the adhesive force.

3. RESULTS AND DISCUSSIONS

Figure 2a shows the temperature-dependent sheet resistance curves of pure ST and all TST films. As shown in this figure, with the increase of annealing temperature, a slow and gradual drop of sheet resistance (R_s) is observed for as-deposited ST film. This is because the ST film has partly crystallized during the sputtering process because of its low T_c (<100 °C). Unlike the *RT* curve for ST, after an initial monotonic decrease, sudden drops of R_s, corresponding to T_c, happen at 175.6, 185.5, and 195.9 °C for $T_{0.32}$ST, $T_{0.43}$ST, and $T_{0.56}$ST, respectively. These values are much higher than that of pure ST and conventional GST (∼150 °C).[12] The high T_c can inhibit the spontaneous crystallization and can make the amorphous state more stable, which is proved in Figure 2b. Figure 2b presents the data retention characteristics for the TST samples. The curves of R_s versus time for all samples at different ambient temperatures are studied, and the failure time is defined as the time required for the R_s falling to half of its initial value at a specific temperature. As shown in the figure, low failure time is obtained with high annealing temperature. By extrapolation from the failure time, on the basis of the Arrhenius law, the maximum fail temperatures after 10 years for $T_{0.32}$ST, $T_{0.43}$ST, and $T_{0.56}$ST films are found to be 79, 92, and 105 °C, respectively, with activation energies (E_a) of 2.1, 2.3, and 2.5 eV. These results are much better than those of ST, and some are even better than those of GST (85 °C, 2.24 eV).[13] In addition, the higher E_a's of TST films mean that they need to overcome a larger energy barrier to achieve the crystallization, which also indicates a stable amorphous state of the TST films.

From the results of Figure 2, we can easily find that, with increasing Ti dopants, the thermal stability of ST is monotonously improved but that the R_s of the initial state increases first and then decreases. To find the reasons, carrier concentrations and mobilities of ST and TST samples are measured by the Hall system, and the results are summarized in Table 1. According to our previous research,[14] after doping ∼6 at. % Ti ($Ti_{0.32}Sb_2Te_3$) in ST, the dramatic reduction in mobility is responsible for the increasing R_s of $Ti_{0.32}$ST film. Adding more Ti, the mobility further reduces by ∼20%; nevertheless, the carrier density increases from 2.32×10^{20} cm^{-3} (for a-$Ti_{0.32}$ST) to 8.26×10^{20} cm^{-3} (for a-$Ti_{0.56}$ST). In the equations of $R = \rho/d$ and $\rho = 1/pq\mu_p$, d is the film thickness, ρ is the resistivity, p is the hole concentration, q is the electric charge, and μ_p is the mobility of the hole. The sharp increase in carrier concentration in turn decreases the initial R_s, as shown in the *RT* curves.

Because the PCM is based on the reversible phase transitions of chalcogenide, the density change between amorphous and crystalline states would affect the device performance. Usually, the crystalline state of phase-change material is more compact, which means that a smaller volume is obtained after Set operation. This will lead to the appearance of void inside the active phase-change area after repeated reversible operations, resulting in the poor contact with electrode. The large density change upon crystallization (∼6.5%) has been considered to be one of the main reasons for the GST-based device failure.[15] Therefore, the densities of both amorphous and crystalline ST and TST films are tested by XRR, and the results are presented in Figure 3. The corresponding XRR simulation is carried out by using GenX software.[16] From Figure 3a, we can see that the XRR plot of ST film becomes quite unsmooth after crystallization, especially as the 2theta is larger than 1.5°. XRR is a technique to reflect a beam of X-rays from a flat surface, and if the interface is perfectly sharp and smooth, then the reflected intensity will obey the Fresnel reflectivity.[17] Thus, the significant difference between curves of as-deposited and crystalline ST film indicates that the mass density changes greatly after further crystallization. After doping more Ti, the plots of crystalline state get more and more smooth. These imply that, with the growth of the crystal nuclei, the surface of

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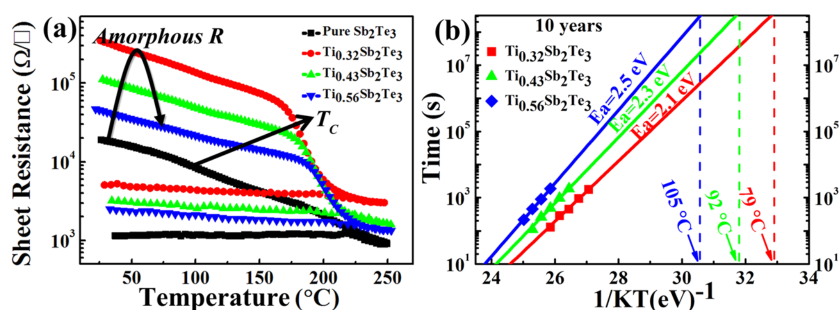

Figure 2. (a) Sheet resistance as a function of annealing temperature for Sb_2Te_3 and TST films. (b) The Arrhenius extrapolation at 10 years of data retention for TST films with different Ti concentrations.

Table 1. Results of Hall Effect Measurements for Pure ST, $Ti_{0.32}Sb_2Te_3$, $Ti_{0.43}Sb_2Te_3$, and $Ti_{0.56}Sb_2Te_3$ Films in Amorphous and Crystalline States

	amorphous			crystalline			
sample	carrier density cm^{-3}	mobility $cm^2\ V^{-1}\ s^{-1}$	Hall coefficient $cm^3\ C^{-1}$	carried density cm^{-3}	mobility $cm^2\ V^{-1}\ s^{-1}$	Hall coefficient $cm^3\ C^{-1}$	type
Sb_2Te_3	7.93×10^{19}	3.96	0.0597	1.42×10^{20}	31.8	0.0431	*P*
$Ti_{0.32}Sb_2Te_3$	2.32×10^{20}	0.416	0.0270	1.50×10^{21}	0.551	0.00415	*P*
$Ti_{0.43}Sb_2Te_3$	4.37×10^{20}	0.316	0.0143	1.64×10^{21}	0.504	0.00381	*P*
$Ti_{0.56}Sb_2Te_3$	8.26×10^{20}	0.258	0.00757	2.73×10^{21}	0.433	0.00229	*P*

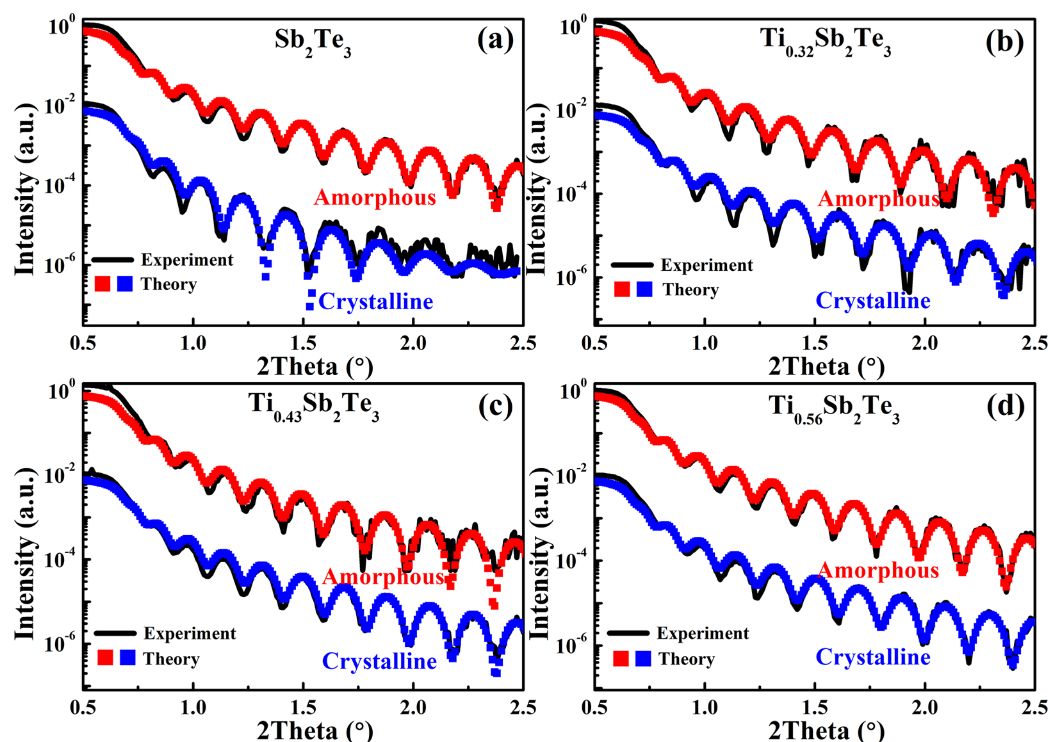

Figure 3. XRR results for (a) Sb_2Te_3, (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ in amorphous and crystalline states. The scatter plots are the corresponding XRR simulation results.

Table 2. Root-Mean-Square Roughness, Thickness, and Mass Density, Extracted from XRR Simulations, for Pure ST, $Ti_{0.32}Sb_2Te_3$, $Ti_{0.43}Sb_2Te_3$, and $Ti_{0.56}Sb_2Te_3$ Films in Amorphous and Crystalline States

	amorphous			crystalline			density
sample	roughness (nm)	thickness (nm)	density ($g{\cdot}cm^{-3}$)	roughness (nm)	thickness (nm)	density ($g{\cdot}cm^{-3}$)	change (100%)
Sb_2Te_3	0.563	42.5	6.00	1.50	38.4	6.45	7.50
$Ti_{0.32}Sb_2Te_3$	0.549	39.9	6.24	1.51	39.1	6.38	2.24
$Ti_{0.43}Sb_2Te_3$	0.708	42.8	6.29	0.621	42.6	6.39	1.59
$Ti_{0.56}Sb_2Te_3$	0.569	42.7	5.85	0.527	42.2	5.93	1.37

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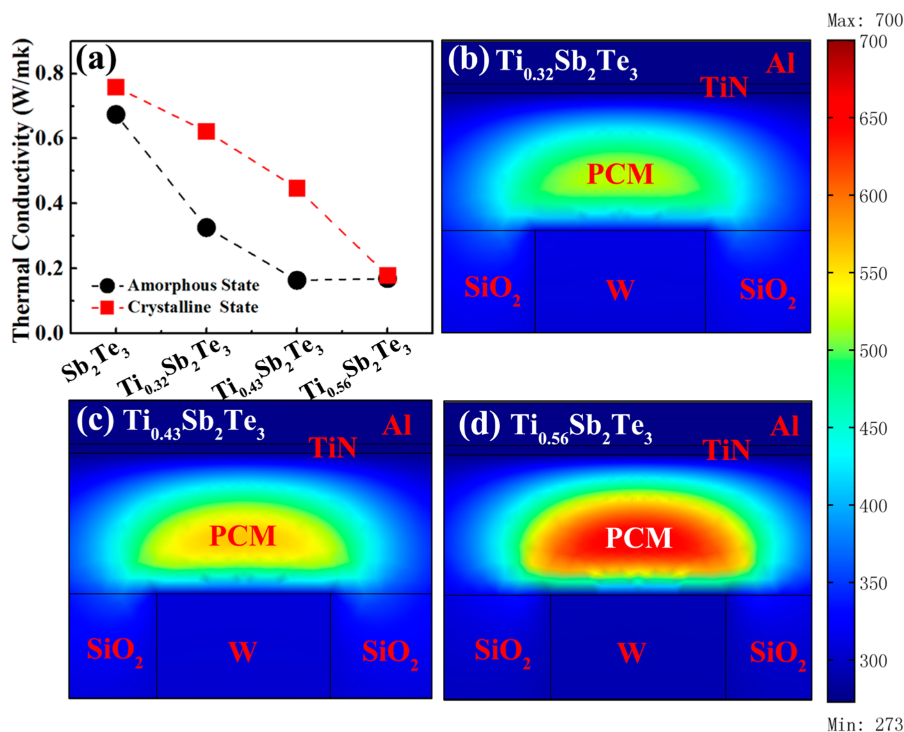

Figure 4. (a) Thermal conductivities of amorphous and crystalline Sb_2Te_3 and TST films. Simulated temperature distributions of phase-change memory cells in Reset state with (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ layers. The temperature unit is k.

ST film gets rougher, but the roughness has been reduced by the incorporation of Ti.

Exact values of the roughness, mass density, and thickness can be obtained from the XRR simulations, as summarized in Table 2. As predicted above, the surface roughness of crystalline ST film almost decreases with increasing Ti concentration. However, the roughnesses for all amorphous samples are found to be fairly similar. The thickness of ST film diminishes a lot after crystallization, and the variation is also dramatically reduced by adding Ti. The mass density of as-deposited ST film is ~6.00 $g\cdot cm^{-3}$ and increases to 6.45 $g\cdot cm^{-3}$ after crystallization. This value is quite consistent with theory density (6.51 $g\cdot cm^{-3}$).[18] The larger mass density of the crystalline state is due to its more ordered atomic arrangement. The densities of amorphous samples slightly increase for $Ti_{0.32}ST$ and $Ti_{0.43}ST$ but decease to 5.85 $g\cdot cm^{-3}$ for $Ti_{0.56}Sb_2Te_3$. This means a possible phase separation of TST alloy with excessive Ti. The density change upon crystallization for ST is 7.50%, and the large volume change would lead to bad contact with the electrode, finally resulting in device failure. After Ti doped, the density change decreases sharply to 2.24% for $T_{0.32}ST$ and continues to decrease moderately with more Ti, which is much lower than that of GST (6.50%[15]). Therefore, the incorporation of Ti in ST can linearly decrease the density change, which would greatly avoid the delamination at phase-change layer/top electrode interface and finally improve the reliability of devices and prolong the lifetime of PCM.

As we all know, phase-change device cells are operated by Joule heat induced from electrical pulse. However, most of the Joule heat diffuses into the surrounding, and a very small part is used for phase transition.[19] Thus, phase-change material with low thermal conductivity is favorable for enhancing energy efficiency. Figure 4a shows the thermal conductivities of ST and TST films. The thermal conductivities of as-deposited and crystalline ST are 0.674 and 0.758 W/mK, respectively, which agree well with those previously reported in the literature (0.50 and 0.78 W/mK, respectively).[20] Such high values would transmit huge heat to the surrounding, which dramatically increases the power consumption. It can be seen that the thermal conductivity of as-deposited ST is much larger than that of as-deposited TST films for its partial crystallization. The values of thermal conductivities decrease to 0.326 and 0.622 W/mK for amorphous and crystalline $T_{0.32}ST$, respectively. With more Ti doping, both values further decrease. For $T_{0.56}ST$, the thermal conductivity of amorphous state (0.169 W/mK) is close to that of crystalline state (0.179 W/mK), which is just a quarter of that for ST and which is also smaller than that for GST (0.18 W/mK for amorphous state, 0.40 W/mK for crystalline state).[19]

To directly explain the effect of the thermal conductivity on the power consumption, a two-dimensional finite analysis[21] is applied to simulate the temperature distributions of the cells during the Reset operation, as shown in Figure 4b–d. It is obvious that, for all cells, the heat generated by the same voltage pulse is concentrated in the active phase-change area on the bottom electrode contact (BEC). The highest temperature is located in the middle of the mushroom-shaped temperature distribution. As the Ti concentration becomes larger, the peak temperature in PCM increases and the temperature of the surrounding decreases. Therefore, because of the decrease of thermal conductivity with Ti doping, the heat dissipation is reduced and most of the Joule heat is used for the phase-change process, which enhances the thermal efficiency and ultimately reduces the power consumption.

Because the phase-change material will be deposited into nanostructure cells in PCM, the performance of devices will be influenced by their morphological and structural characteristics. A small grain size will benefit improving the gap-fill capability, in turn promoting the device manufacturing. Therefore, the grain sizes of crystalline ST and TST films are also studied by

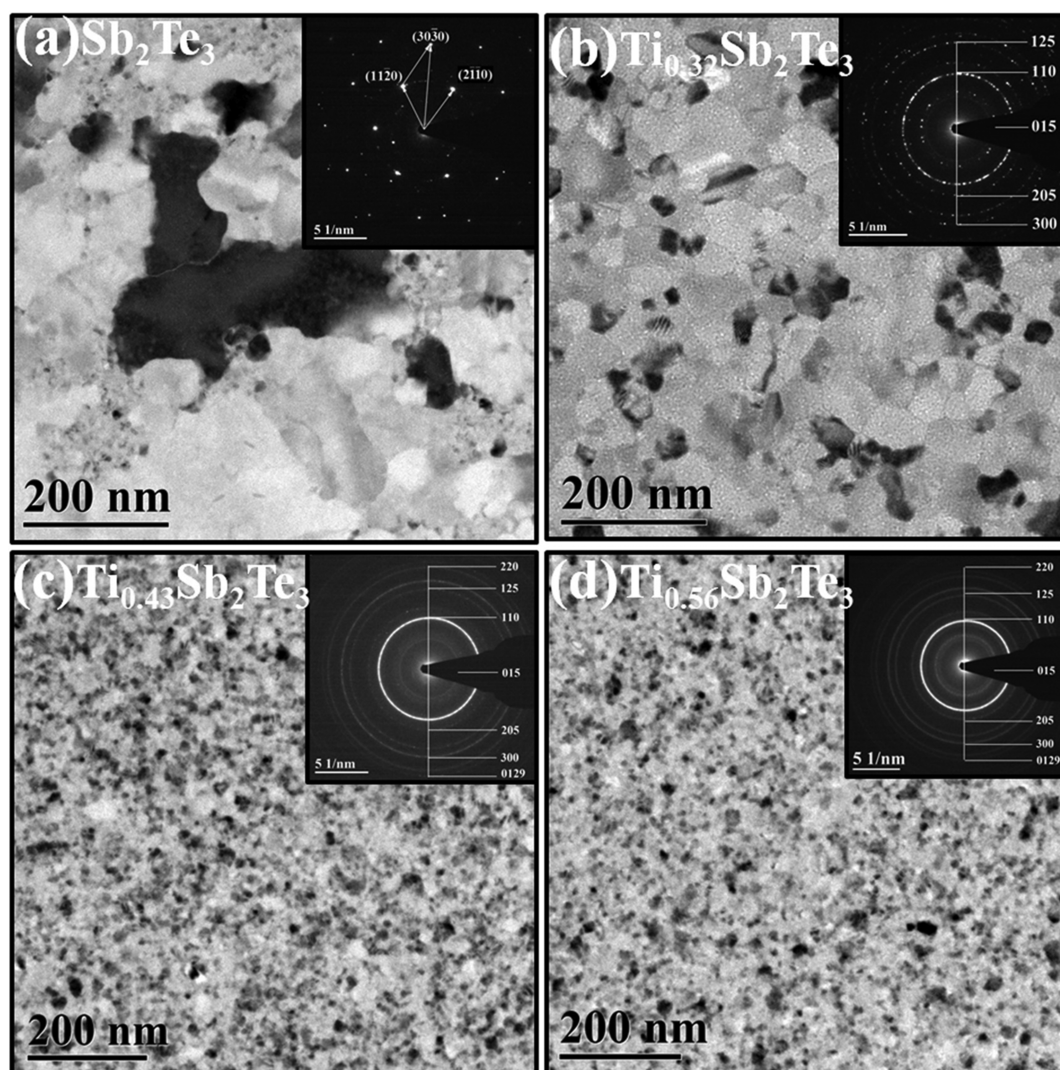

Figure 5. TEM images of (a) Sb_2Te_3, (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ films after annealing at 250 °C. The corresponding SAED patterns are exhibited in the insets.

TEM, as shown in Figure 5. From Figure 5a, we can see that crystalline ST film has irregular shape gains, and their sizes are several hundred nanometers. As we know, large grain size can lead to poor adhesion between the phase-change film and substrate, which means that ST films would easily fall off from the wafer during the PCM preparation process. In the case of $Ti_{0.32}$ST, the shape of grain changes to polygon, and the size obviously decreases to ~50 nm (as shown in Figure 5b). With larger Ti concentration, the grain size further decreases to ~15 nm for $Ti_{0.43}$ST and to ~12 nm for $Ti_{0.56}$ST. This variation can also be confirmed by the comparison of corresponding selected area electron diffraction (SAED) patterns. The more continuous the diffraction rings are, the smaller the grain size is.[22] As shown in the inset, the single crystal-like diffraction spots for ST suggest that the grain size is larger than 180 nm. However, for all TST films, the corresponding SAED patterns are polycrystalline rings, but the continuities of these rings are much different. The concentric rings of $Ti_{0.32}$ST are intermittent and become almost continuous for $Ti_{0.43}$ST (with several scattering spots). In the case of $Ti_{0.56}$ST, these rings are fully continuous. Thus, the grain size of ST diminishes with the increase of Ti concentration, which will improve gap-fill capability for high aspect ratio structures and which will make the fabrication of the PCM device much easier. Furthermore, since small grains have higher interface/volume ratios, they can generate more free carriers, resulting in a faster crystallization rate.[23]

To investigate the influence of these factors on phase-change characteristics, PCM test cells based on ST and TST films are manufactured and tested. Figure 6 shows the resistance−voltage curves with different electrical pulse widths. From Figure 6a, we can see that ST-based PCM cells have a high resistance larger than 10^6 Ω and a resistance ratio of about 3 orders of magnitude. The cells can be reversibly switched by using 10 ns width pulses. All the values of pulse widths in this work are the set values of the pulse generator. Affected by the parasitic capacitance in the test circuit, the actual pulse width across the cells is a few broader than the ideal one, accompanied by a series of subpulses (as shown in Figures S1−S5 of the Supporting Information). For all TST-based PCM devices, as exhibited in Figure 6b−d, 10 ns is also enough to achieve the entirely crystalline−amorphous operations. This means that, with better thermal stability, PCM cells using TST alloy are more suitable for DRAM-like PCM application than ST-based ones. Because of the limitation of the maximum output frequency of our pulse generator, the narrowest

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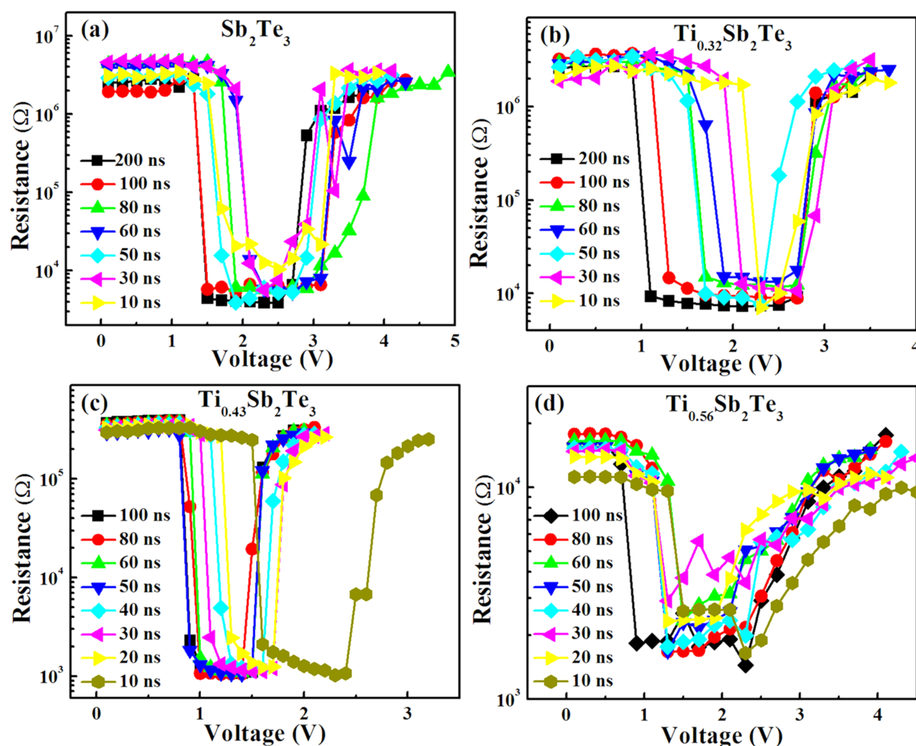

Figure 6. Resistance−voltage curves for PCM test cells based on (a) Sb_2Te_3, (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ films.

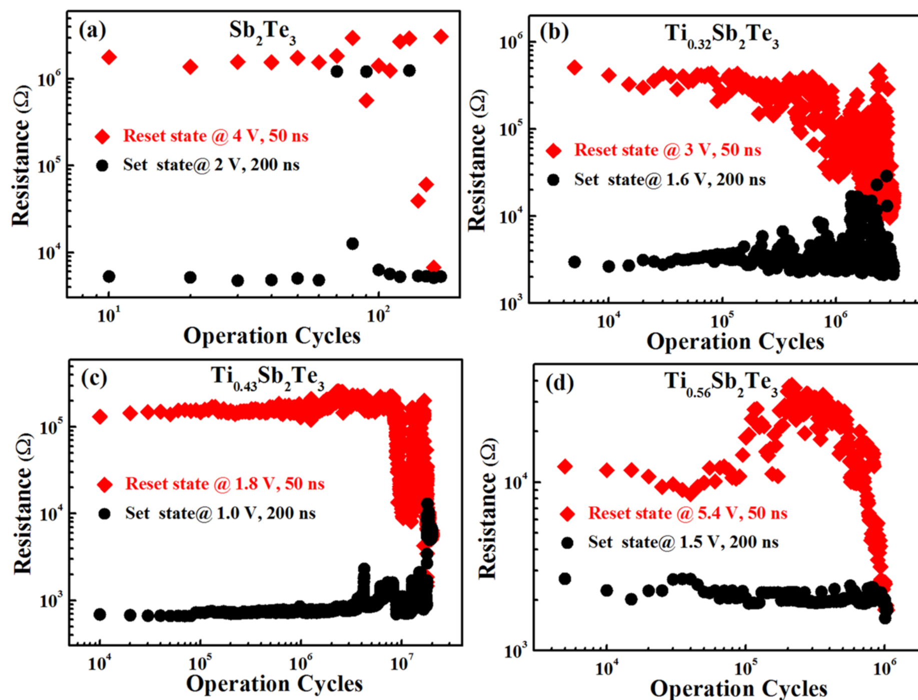

Figure 7. Endurance characteristics of PCM test cells based on (a) Sb_2Te_3, (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ films.

measurable square-wave voltage pulse is around 10 ns. For this reason, we are not able to further know the effect of Ti concentration on the crystallization speed of ST. However, the incorporation of Ti in ST indeed affects other electrical properties, such as resistance ratio and operation voltages. For $Ti_{0.32}$ST-based PCM cell, the resistance ratio between high and low resistances is ∼400, half as large as that of the ST-based one. With higher Ti concentration, as shown in Figure 6c, the ratio further decreases to ∼300, but it still can provide distinguishable high/low resistances for PCM application. In the case of the $Ti_{0.56}$ST-based PCM cell, the high resistance is just one order larger in magnitude than the low one. This variation trend of resistance is almost the same as the results of the *RT* experiment (Figure 2a), except for the ST-based PCM cell. This is because the ST film used in *RT* experiment is an as-deposited state that has partly crystallized. From a previous Hall

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analysis, we know that the increasing carrier concentration after adding more Ti is responsible for the changes of the device's resistances.

In addition, the voltages required to switch the cells are also changed with Ti content. Pulses with amplitudes exceeding 3 V are needed to reset the ST-based PCM cells, while ~2.8 V is enough for $Ti_{0.32}$ST ones. For $T_{0.43}$ST-based ones, the Reset voltages further decrease to ~1.8 V, almost 50% smaller compared to cells using ST films. As discussed in Figure 4, thermal conductivity of ST monotonously decreases with the increase of Ti content; therefore, the heat dissipation is reduced and the thermal efficiency is enhanced. This is one of the major reasons for the decrease of Reset operation voltages. Nevertheless, only by applying voltage pulses larger than 3.5 V can the $T_{0.56}$ST-based cells complete the switch from low-resistance state to high-resistance state. According to our previous research,[24] doping too much Ti in ST (>10.3 at. %) will cause the phase separation after endurance operations. Therefore, the inhomogeneous phase of $Ti_{0.56}$ST after repeated operations is the possible reason for the larger operation voltages. The conclusion is also supported by the bad uniformity of $T_{0.56}$ST-based PCM array cells (Figure S6 of the Supporting Information), which is much worse than those of $T_{0.32}$ST and $T_{0.43}$ST-based ones (Figures S7 and S8 of the Supporting Information).

Next, endurance characteristics of these device cells are also investigated, as shown in Figure 7. ST-based PCM cells can just be repeatedly operated less than 60 times and then are stuck in the high-resistance state, which is called Reset-Stuck. This failure type is induced by the delamination at the phase-change film/top electrode interface after repeated operations,[25] which is caused by the large density change (>7.5%, as shown in Table 2) and big grain size (>200 nm, as shown in Figure 5) of ST film. Also, large pulse amplitudes (4 V/2 V) are needed to maintain the stable high/low resistance states, which are also harmful to the device life. It can be seen clearly that the cycle life is greatly prolonged by using TST films, as presented in Figure 7b−d. Cycles exceeding 10^6 times are obtained for TST-based devices, and even 10^7 times is found for the $Ti_{0.43}$ST-based one, which is still a good result compared to that of a device using GST film under laboratory conditions (10^6~10^7 cycles).[26] Before failure, $Ti_{0.32}$ST and $Ti_{0.43}$ST-based PCM cells can maintain quite stable resistance ratios of 2 orders of magnitude. The uniform structure, less density change, and smaller grain size of TST films are responsible for the good endurance characteristics of these PCM cells, and the lower thermal conductivity is the main reason for the lower required operation voltages. Although the $Ti_{0.56}$ST cell can also be repeatedly operated around 10^6 cycles, its low resistance ratio, unstable resistance, and high operation voltages make it unsuitable for DRAM-like PCM application. Thus, $Ti_xSb_2Te_3$ alloy with x between 0.4 and 0.5 seems to be a good candidate for fast-switching and high-endurance PCM applications. As the dimension further scales down, accompanied with sharply reduced program energy, TST-based cell life would be exponentially prolonged,[27] which has potential to meet the stringent requirement for DRAM-like applications.

4. CONCLUSIONS

Owing to growth-dominated crystallization mechanism, ST-based PCM test cells are found to possess 10 ns operation rate, which is much faster than conventional GST (~50 ns). However, its really poor thermal stability (spontaneous crystallization during the deposited process) makes it unsuitable to be applied in PCM. Besides, too high thermal conductivities of ST (0.674 and 0.758 W/mK for as-deposited and crystalline states, respectively) lead to a larger amount of heat dissipation to the surrounding, which in turn increases the required operation voltages and power consumption. Also, a quite large density change of ST film after crystallization (>7.5%), together with ~200 nm big grains, sharply shortens the cycle life of PCM devices (<100 cycles).

These drawbacks of ST are effectively overcome by adding Ti, called Ti−Sb−Te alloy, without degrading its fast switching speed. $Ti_{0.32}$ST already has a data retention of 79 °C@10-year, and better thermal stability can be obtained with higher Ti concentration. Besides, the density variation between amorphous and crystalline states is distinctly reduced below 2.24% for $Ti_{0.32}$ST and further to 1.37% for $Ti_{0.56}$ST, which would greatly reduce the possibility of bad contact with electrode and which would ultimately prolong the lifetime of a PCM device. The dramatic refinement of grain sizes (below 50 nm) resulting from doped Ti not only improves the adhesive force between the phase-change film and substrate but also speeds up the crystallization process. Furthermore, as the Ti concentration increases, the thermal conductivities of both amorphous and crystalline states decrease monotonically, which helps to enhance the thermal efficiency.

Our TST-based test chips (with ~200 nm tungsten-heating electrode) have demonstrated 10 ns operation speed and ~10^6 cycling endurance. The Ti content of TST affects both resistance ratio and required voltages for Reset operations. The resistance ratio of TST decreases with the increase of Ti concentration. Compared to ST-based PCM cells, the required voltages for $Ti_{0.32}$ST-based ones are slightly reduced, while ~50% reduction is found for $Ti_{0.43}$ST-based ones. However, in the case of $Ti_{0.56}$ST-based cells, the device performances get worse, including high operation voltages, too small resistance ratio, unstable resistance, and bad uniformity, which may be due to the phase separation after excessive Ti-doping. Therefore, $Ti_xSb_2Te_3$ materials with x between 0.4 and 0.5 are the optimal components to ensure good overall properties of TST-based PCM.

ASSOCIATED CONTENT

Supporting Information

Figure S1 shows the schematic picture of the electrical test setup. Figures S2−S5 show the waveforms of the voltage pulses (10−200 ns) from the pulse generator and across the device cell. Figures S6−S8 show the uniformity of $Ti_{0.32}$ST, $Ti_{0.43}$ST, and $Ti_{0.56}$ST based PCM devices, respectively. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Notes

The authors declare no competing financial interest.

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